A quick introduction to the Intel® Xeon Phi™

Stephen Blair-Chappell, Intel
What is it?

• Co-processor
  – PCI Express card
  – Stripped down Linux operating system (busybox/dash)

• Dense, simplified processor
  – Simplifications for power savings In-order
  – Wider vector unit
  – Wider hardware thread count

• Lots of names
  – Many Integrated Core architecture, aka MIC
  – Knights Corner (code name)
  – Intel Xeon Phi Co-processor SE10P (product name)
Intel® Xeon Phi™ Architecture Overview

- **Cores:** 61 cores, at 1.1 GHz in-order, support 4 threads
- **512 bit Vector Processing Unit**
- **32 native registers**

**Reliability Features:**
- Parity on L1 Cache, ECC on memory
- CRC on memory IO, CAP on memory IO

**High-speed bi-directional ring interconnect**

**Fully Coherent L2 Cache**

**8 memory controllers**
- 16 Channel GDDR5 MC
- PCIe GEN2
Core Architecture Overview

60+ in-order, low power IA cores in a ring interconnect

Two pipelines
- Scalar Unit based on Pentium® processors
- Dual issue with scalar instructions
- Pipelined one-per-clock scalar throughput

SIMD Vector Processing Engine
- 4 hardware threads per core
  - 4 clock latency, hidden by round-robin scheduling of threads
  - Cannot issue back to back inst in same thread

Coherent 512KB L2 Cache per core
Key Differentiators
Xeon Phi vs Workstation

More Cores
Slower Clock Speed
Wider SIMD registers
Faster Bandwidth
In-order pipeline
## A Tale of Two Architectures

<table>
<thead>
<tr>
<th>Feature</th>
<th>Intel® Xeon® processor</th>
<th>Intel® Xeon Phi™ Coprocessor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sockets</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>Clock Speed</td>
<td>2.6 GHz</td>
<td>1.1 GHz</td>
</tr>
<tr>
<td>Execution Style</td>
<td>Out-of-order</td>
<td>In-order</td>
</tr>
<tr>
<td>Cores/socket</td>
<td>8</td>
<td>Up to 61</td>
</tr>
<tr>
<td>HW Threads/Core</td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>Thread switching</td>
<td>HyperThreading</td>
<td>Round Robin</td>
</tr>
<tr>
<td>SIMD widths</td>
<td>8SP, 4DP</td>
<td>16SP, 8DP</td>
</tr>
<tr>
<td>Peak Gflops</td>
<td>692SP, 346DP</td>
<td>2020SP, 1010DP</td>
</tr>
<tr>
<td>Memory Bandwidth</td>
<td>102GB/s</td>
<td>320GB/s</td>
</tr>
<tr>
<td>L1 DCache/Core</td>
<td>32kB</td>
<td>32kB</td>
</tr>
<tr>
<td>L2 Cache/Core</td>
<td>256kB</td>
<td>512kB</td>
</tr>
<tr>
<td>L3 Cache/Socket</td>
<td>30MB</td>
<td>none</td>
</tr>
</tbody>
</table>
Theoretical Peak Flops Performance Example

Two socket Intel® Xeon® E5-2670 Processor

<table>
<thead>
<tr>
<th>Freq</th>
<th>Sockets</th>
<th>Num Cores</th>
<th>Vector Width</th>
<th>FP Ops</th>
<th>GFlops</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.6</td>
<td>2</td>
<td>8</td>
<td>4</td>
<td>2</td>
<td>666</td>
</tr>
</tbody>
</table>

Single card Xeon Phi Coprocessor (B0)

<table>
<thead>
<tr>
<th>Freq</th>
<th>Sockets</th>
<th>Num Cores</th>
<th>Vector Width</th>
<th>FP Ops</th>
<th>GFlops</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.091</td>
<td>1</td>
<td>61</td>
<td>16</td>
<td>2 (using FMA)</td>
<td>2,128</td>
</tr>
</tbody>
</table>

x3.20
**Synthetic Benchmark Summary (Intel® MKL)**

**SGEMM** (GF/s)

- **Up to 2.9X** Lower is Better
- **1,729**
- **Up to 85% Efficient**
- **1,860**
- **86% Efficient**

**DGEMM** (GF/s)

- **Up to 2.8X** Lower is Better
- **833**
- **82% Efficient**
- **883**
- **82% Efficient**

**SMP Linpack** (GF/s)

- **Up to 2.6X** Lower is Better
- **722**
- **71% Efficient**
- **803**
- **75% Efficient**

**STREAM Triad** (GB/s)

- **Up to 2.2X** Lower is Better
- **159**
- **ECC On**
- **174**
- **ECC On**

Coprocessor results: Benchmark run 100% on coprocessor, no help from Intel® Xeon® processor host (aka native)

Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products.

Source: Intel Measured results as of October 26, 2012  Configuration Details: Please reference slide speaker notes.

For more information go to [http://www.intel.com/performance](http://www.intel.com/performance)
# Intel® Xeon Phi™ Coprocessor:
**Increases Application Performance up to 10x**

<table>
<thead>
<tr>
<th>Segment</th>
<th>Customer</th>
<th>Application</th>
<th>Performance Increase(^1) vs. 2S Xeon*</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Energy</strong></td>
<td>Acceleware</td>
<td>8th order isotropic variable velocity</td>
<td>Up to 2.23x</td>
</tr>
<tr>
<td></td>
<td>Sinopec</td>
<td>Seismic Imaging</td>
<td>Up to 2.53x(^2)</td>
</tr>
<tr>
<td></td>
<td>CNPC (China Oil &amp; Gas)</td>
<td>GeoEast Pre-Stack Time Migration (Seismic)</td>
<td>Up to 3.54x(^2)</td>
</tr>
<tr>
<td><strong>Financial Services</strong></td>
<td>Financial Services</td>
<td>BlackScholes SP</td>
<td>Up to 7.5x</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Monte Carlo SP</td>
<td>Up to 10.75x</td>
</tr>
<tr>
<td><strong>Physics</strong></td>
<td>Jefferson Labs</td>
<td>Lattice QCD</td>
<td>Up to 2.79x</td>
</tr>
<tr>
<td><strong>Finite Element</strong></td>
<td>Sandia Labs</td>
<td>miniFE (Finite Element Solver)</td>
<td>Up to 2x(^3)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Up to 1.3x(^5)</td>
</tr>
<tr>
<td><strong>Solid State Physics</strong></td>
<td>ZIB (Zuse-Institut Berlin)</td>
<td>Ising 3D (Solid State Physics)</td>
<td>Up to 3.46x</td>
</tr>
<tr>
<td><strong>Digital Content Creation/Video</strong></td>
<td>Intel Labs</td>
<td>Ray Tracing (incoherent rays)</td>
<td>Up to 1.88x(^4)</td>
</tr>
<tr>
<td></td>
<td>NEC</td>
<td>Video Transcoding</td>
<td>Up to 3.0x(^2)</td>
</tr>
<tr>
<td><strong>Astronomy</strong></td>
<td>CSIRO/ASKAP (Australia Astronomy)</td>
<td>tHogbom Clean (Astronomy image smear removal)</td>
<td>Up to 2.27x</td>
</tr>
<tr>
<td></td>
<td>TUM (Technische Universität München)</td>
<td>SG++ (Astronomy Adaptive Sparse Grids/Data Mining)</td>
<td>Up to 1.7x</td>
</tr>
<tr>
<td><strong>Fluid Dynamics</strong></td>
<td>AWE (Atomic Weapons Establishment - UK)</td>
<td>Cloverleaf (2D Structured Hydrodynamics)</td>
<td>1.77x</td>
</tr>
</tbody>
</table>

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**Notes:**
1. 2S Xeon\(^*\) vs. 1 Xeon Phi\(^*\) (preproduction HW/SW & Application running 100% on coprocessor unless otherwise noted)
2. 2S Xeon\(^*\) vs. 2S Xeon\(^*\) + 2 Xeon Phi\(^*\) (offload)
3. 8 node cluster, each node with 2S Xeon\(^*\) (comparison is cluster performance with and without 1 Xeon Phi\(^*\) per node) (Hetero)
5. 8 node cluster, each node with 2S Xeon\(^*\) (comparison is cluster performance with Xeon only vs. Xeon Phi \(^*\) only (1 Xeon Phi \(^*\) per node) (Native)

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Programming Models and Mindsets

Multi-Core Centric
- Xeon
- Multi-Core Hosted
  - General purpose serial and parallel computing
- Offload
  - Codes with highly-parallel phases
- Main()
- Foo()
- MPI_*()
- Multi-Core Hosted
  - Highly-parallel codes
- Many-Core Hosted
  - MIC
- Many-Core Centric
- Symmetric
  - Codes with balanced needs
- Main()
- Foo()
- MPI_*()

Range of models to meet application needs

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Examples of Offloading

C/C++ Offload Pragma

```c
#pragma offload target (mic)
#pragma omp parallel for reduction(+:pi)
for (i=0; i<count; i++) {
    float t = (float)((i+0.5)/count);
    pi += 4.0/(1.0+t*t);
}
pi /= count;
```

MKL Implicit Offload

//MKL implicit offload requires no source code changes, simply link with the offload MKL Library.

MKL Explicit Offload

```c
#pragma offload target (mic) \
    in(transa, transb, N, alpha, beta) \
    in(A:length(matrix_elements)) \
    in(B:length(matrix_elements)) \
    in(C:length(matrix_elements)) \
    out(C:length(matrix_elements)alloc_if(0))
    sgemm(&transa, &transb, &N, &N, &N, &alpha, 
        A, &N, B, &N, &beta, C, &N);
```

Fortran Offload Directive

```fortran
!dir$ omp offload target(mic)
!omp parallel do
    do i=1,10
        A(i) = B(i) * C(i)
    enddo
!omp end parallel
```

C/C++ Language Extensions

```c
class _Shared common { 
    int data1;
    char *data2;
    class common *next;
    void process();
};

_Shared class common obj1, obj2;
...
_Cilk_spawn _Offload obj1.process();
_Cilk_spawn obj2.process();
...
Knights Landing is the code name for the 2nd generation product in the Intel® Many Integrated Core Architecture.

Knights Landing targets Intel’s 14 nanometer manufacturing process.

Knights Landing will be productized as a processor (running the host OS) and a coprocessor (a PCIe endpoint device).

Knights Landing will feature on-package, high-bandwidth memory.

Flexible memory modes for the on package memory include: flat, cache, and hybrid modes.

Intel® Advanced Vector Extensions AVX-512
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