RECAP

Adrian Jackson

adrianj@epcc.ed.ac.uk

Xeon Phi Processor

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8 memory controllers
16 Channel GDDR5 MC
PCIe GEN2

PCIe Client Logic

GDDR MC
GDDR MC

Cores: 61 core s, at 1.1 GHz
in-order, support 4 threads
512 bit Vector Processing Unit
32 native registers

Core L2   Core L2   Core L2   Core L2

TD   TD   TD   TD

TD   TD   TD   TD

GDDR MC
GDDR MC

L2   L2   L2   L2

Core   Core   Core   Core

High-speed bi-directional
ring interconnect
Fully Coherent L2 Cache

Reliability Features
Parity on L1 Cache, ECC on memory
CRC on memory IO, CAP on memory IO

Xeon Phi

- 60 cores -> 240 threads
  - 120 or above required for instruction issuing

- Two different programming models
  - Offload, native
  - OpenMP and MPI (also Cilk, OpenCL)
  - Also can use libraries to do the same (i.e. MKL)

- Accelerator card
  - Same as GPU, restrict data transfers for good performance

Xeon Phi

- Xeon Phi hardware has potential for high peak performance
  - Particularly at single precision
- Achievable performance generally lower
  - Especially if memory or communication bound
- Full vectorisation and FMA essential for highest performance
  - Can still get good performance without
- Good memory re-use essential for highest performance
  - Same as for normal CPU code